

wherein the graphics processor is programmed to render at least one or more portions of said 3D polygon-based graphic objects for displaying on said display device.

207. A home video game system as in claim 206 wherein the graphics processor is a coprocessor that is responsive to specific instructions used for rendering 3D objects.

208. A home video game system as in claim 206 wherein the graphics processor is a pipelined processor.

209. A home video game system as in claim 206 wherein the graphics processor is a programmable pipelined processor.

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210. A home video game system as in claim 206 wherein the graphics processor includes embedded RAM cache memory.

211. A home video game system as in claim 206 wherein the circuitry for accelerating 3D graphic special transformation operations includes a high speed multiplier for performing computations for performing rotation and/or scaling of a 3D graphic object or portions of the object to be displayed.

212. A home video game system as in claim 206 wherein the graphics processor includes at least an Arithmetic Logic Unit and a multiplier circuit for performing computations for rotation and/or scaling of a polygon-based graphic object to be displayed.

213. A home video game system as set forth in claim 212 wherein the multiplier performs multiply operations using at least 16-bit length operands.

214. A home video game system as in claim 206 wherein the graphics processor is programmed to rotate an array of data corresponding to polygon vertex points.

215. A home video game system as in claim 206 wherein two or more polygon-based graphic objects are displayed simultaneously.

216. A home video game system as in claim 206 wherein the graphics processor is programmed to perform texture mapping operations.

217. A home video game system as in claim 206 wherein the graphics processor includes a pixel plotting circuit for converting display screen pixel coordinate addresses to a character map address format.

218. A home video game system as in claim 206 having a set of instructions for programming the graphics processor unit for rendering 3D objects wherein the instruction set includes an instruction for controlling transparency of a displayed object.

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219. A home video game system as in claim 206 having a set of instructions for programming the graphics processor unit wherein the instruction set includes a fractional signed multiply instruction for computing gradients and/or slopes for rotating polygon-based displayed objects.

220. A home video game system as in claim 206 wherein the graphics processor incorporates at least an Arithmetic Logic Unit and cache RAM fabricated on a single chip.

221. A home video game system as in claim 206 wherein the graphics processor incorporates at least an Arithmetic Logic Unit and a high speed multiplier circuit fabricated on a single chip.

222. A home video game system as in claim 206 wherein the graphics processor comprises an Arithmetic Logic Unit, a multiplier unit and plurality of registers fabricated on a single chip.